CLAIMS

What is claimed is:

1. An apparatus for executing application programming at reduced circuit power consumption levels, comprising:

(a) a processing element; and

(b) means for modulating the clock speed of said processing element under the control of an application program executable on said processing element.

2. An apparatus as recited in claim 1, wherein the clock speed modulation means under program control is configured to allow the selection of at least two clock speeds.

3. An apparatus as recited in claim 1, wherein the clock speed modulation means comprises a divider circuit configured to divide an incoming oscillator signal which is received by said processing element and from which processor clock speed is derived.

4. An apparatus as recited in claim 3, wherein the divider circuit is configured to divide the incoming oscillator signal by a value greater than unity, such that the oscillator signal provided to the processor is less than the incoming oscillator frequency.

5. An apparatus as recited in claim 4, wherein the divider circuit is configured to have at least one discrete division value that may be selected by the executing program.

6. An apparatus as recited in claim 5, wherein the incoming oscillator signal may be divided by eight under program direction and supplied to the processing element.

7. An apparatus as recited in claim 3, wherein the divider circuit is configured to divide the incoming oscillator signal by a value less than unity, wherein the oscillator signal provided to the processor is greater than the incoming oscillator frequency.

8. An apparatus as recited in claim 7, wherein the divider circuit is configured with at least one discrete division value that may be selected by the executing program.

9. An apparatus as recited in claim 8, wherein the incoming oscillator signal may be divided by one-half under program direction, wherein the speed of the oscillator signal supplied to the processing element is therefore doubled.

10. An apparatus as recited in claim 1, wherein the clock speed modulation means comprises a circuit configured to select an alternative oscillator signal for the processing element.

11. An apparatus as recited in claim 10, wherein the alternative oscillator signal comprises a lower frequency oscillator that is otherwise utilized for driving a real-time clock circuit.

12. An apparatus as recited in claim 11, wherein the alternative oscillator is at a frequency of less than 100 kHz.

13. An apparatus as recited in claim 11, wherein the alternative oscillator is at a frequency of approximately 32 kHz.

14. An apparatus as recited in claim 1, wherein the clock speed modulation means is integrated within the processing element.

15. An apparatus as recited in claim 1, further comprising:

(a) means for modifying the duration of peripheral device chip selects being output by said processing element; and

(b) said chip select duration modifying means configured to change duration of at least one chip select signal in response to the selected clock speed of the processor such that peripheral access timing requirements are met while limiting the power consumption of the peripheral device associated with device selection.

16. An apparatus as recited in claim 15, wherein the chip select duration modification means comprises a digital circuit which receives processor timing signals and at least one conventional chip select signal from which it generates a power-saving chip select signal having a relative duration which is responsive to changes in processor clock speed.

17. An apparatus as recited in claim 16, wherein the digital circuit for modifying chip select duration comprises a timing circuit triggered by a processor timing signal.

18. An apparatus as recited in claim 16, wherein the digital circuit for modifying chip select duration comprises latching circuitry for sufficiently retaining data integrity according to the timing of the power-saving chip select signal.

19. An apparatus as recited in claim 15, wherein the chip select duration modification means is integrated within said processing element.

20. In a processing element configured for operation at a clock speed as derived from an oscillator, wherein the improvement comprises:

(a) an oscillator frequency modification circuit;

(b) said oscillator frequency modification circuit being configured to modify the frequency received by the processing element as an execution clock; and

(c) said oscillator frequency modification circuit is configured to respond to the programmed instructions executing on said processing element to allow changing processor execution speed.

21. In the processing element as recited in claim 20, wherein the processing element is an electronic circuit or device capable of executing programmed instructions as selected from the group of devices and circuits consisting of microprocessors, microcontrollers, digital-signal processors, and central processing units.

22. In the processing element as recited in claim 20, wherein the oscillator frequency modification circuit comprises a selective oscillator divider circuit which divides an incoming oscillator signal under program control to be utilized as the clock within the processing element.

23. In the processing element as recited in claim 22, wherein the selective oscillator divider is configured to divide the incoming oscillator signal by a value greater than unity when directed by the executing program, such that the clock speed of the processing element may be reduced.

24. In the processing element as recited in claim 22, wherein the selective oscillator divider is configured to divide the incoming oscillator signal by a value less than unity when directed by the executing program, such that the clock speed of the

processing element may be increased.

25. In the processing element as recited in claim 20, wherein the oscillator frequency modification circuit comprises an oscillator selection circuit configured to allow the selection of at least one alternative oscillator under program control to be utilized as the clock within the processing element.

26. In the processing element as recited in claim 20, wherein the oscillator frequency modification circuit is integrated within the processing element.

27. In an electronic circuit containing a processor element configured for operation at more than one clock frequency, and to which chip select outputs are interfaced to peripheral devices, wherein the improvement comprises:

(a) a chip select timing circuit which generates a signal in response to processor element clock frequency and timing; and

(b) a gating circuit which receives a signal from said chip select timing circuit and in response alters the percentage interval over which chip select outputs to the peripheral devices are active.

28. In the electronic circuit as recited in claim 27, wherein the processing element is an electronic circuit or device capable of executing programmed instructions as selected from the group of devices and circuits consisting of microprocessors,

microcontrollers, digital-signal processors, and central processing units.

29. In the electronic circuit as recited in claim 27, wherein the peripheral devices comprise memory devices.

30. In the electronic circuit as recited in claim 29, wherein the memory devices comprise static memory integrated circuits.

31. In the electronic circuit as recited in claim 27, wherein the electronic circuit comprising the chip select timing circuit and gating circuit are integrated within a processing element.

32. A circuit for modulating the duration of chip select signals in association with a processor element capable of operating with a selectable cycle clock, comprising:

(a) a processor clock speed detection circuit;

(b) a chip selection restriction circuit connected to said clock speed detection circuit;

(c) said chip selection restriction circuit receiving one or more signals associated with said processor element and configured to generate a restricted chip select signal in response to processor clock speed; and

(d) a chip select gating circuit which receives said restricted chip select signal for modulating at least one chip select output signal to at least one peripheral device of

the processing element.

33. A circuit as recited in claim 32, wherein said chip selection restriction circuit is configured to generate an output responsive to selected periods of the oscillator clock within a given instruction cycle.

34. A circuit as recited in claim 33, wherein the selected periods of said oscillator clock comprise a given multiple of periods at a predetermined position within a given instruction cycle.

35. A circuit as recited in claim 34, wherein selected periods comprise the last two periods within a given instruction cycle.

36. A circuit as recited in claim 32, wherein said chip selection restriction circuit is configured with a timer circuit that generates a signal of predetermined duration as triggered by a processor signal.

37. A circuit as recited in claim 36, wherein the timer circuit is triggered by an output enable signal from the processor element.

38. A circuit as recited in claim 32, wherein the chip select gating circuit logically combines said restricted chip select signal to conventional peripheral chip

select signals to generate new power-saving peripheral chip selects whose relative duration is responsive to processor clock speed.

39. A circuit as recited in claim 38, wherein the logical combination comprises ANDing of a conventional chip select signal with that of the restricted chip select signal to generate the new power-saving peripheral chip select.

40. A circuit for reducing the operating current for devices which interface to a processing element that utilizes a selectable frequency processor clock, comprising:

(a) a chip select timing circuit which interfaces with said processing element;

(b) said chip select timing circuit receiving at least one signal indicative of the selected frequency of the processor clock;

(c) said chip select timing circuit receiving at least one timing conditioning signal;

(d) said chip select timing circuit logically combining said received signals into a chip select restriction signal;

(e) a gating circuit which utilizes the chip select restriction signal to gate at least one received chip select signal; and

(f) said gating circuit generating altered chip select signals that have a timing and pulse width configured in response to processor element clock speed.

41. A circuit as recited in claim 40, wherein the signal indicative of the selected frequency of the processor clock comprises a division value.

42. A circuit as recited in claim 40, wherein the processing element is configured for a selectable frequency processor clock by dividing a received clock signal for use as a cycle clock.

43. A circuit as recited in claim 40, wherein the processing element is configured for a selectable frequency processor clock by multiplying a received clock signal for use as a cycle clock to thereby scale up the normal speed of the processor clock.

44. A circuit as recited in claim 40, wherein the processing element is configured for a selectable frequency processor clock to allow the selection of an alternate oscillator input to drive the processor clock.

45. A circuit as recited in claim 44, wherein the alternate oscillator is configured as a low frequency oscillator.

46. In an electronic circuit containing a processor element configured for operation at more than one clock frequency, and to which chip select outputs are interfaced to peripheral devices, wherein the improvement comprises:

a chip select timing circuit which generates a signal in response to processor element clock frequency and timing; and

a gating circuit which receives a signal from said chip select timing circuit and in response alters the percentage interval over which chip select outputs to the peripheral devices are active.

47. In the electronic circuit as recited in claim 46, wherein the processing element is an electronic circuit or device capable of executing programmed instructions as selected from the group of devices and circuits consisting of microprocessors, microcontrollers, digital-signal processors, and central processing units.

48. In the electronic circuit as recited in claim 46, wherein the peripheral devices comprise memory devices.

49. In the electronic circuit as recited in claim 46, wherein the memory devices comprise static memory integrated circuits.

50. A method of reducing power consumption within a processing element receiving an oscillator signal for driving its clock speed, comprising:

generating a processor clock speed control signal in response to programmed instructions being executed on said processing element; and

modifying the frequency of the oscillator signal in response to said processor

clock speed signal.

51. A method as recited in claim 50, wherein the modification of the frequency of the oscillator signal comprises dividing the incoming oscillator frequency.

52. A method as recited in claim 50, wherein the modification of the frequency of the oscillator signal comprises multiplying the incoming oscillator frequency.

53. A method as recited in claim 50, wherein the modification of the frequency of the oscillator signal comprises selecting an alternative oscillator to be utilized by the processor element for driving the clock speed.

54. A method of reducing power consumption in a circuit containing a processing element configured for multiple clock speed operation which is interfaced to peripheral devices, comprising:

generating a processor speed selection signal that is responsive to the selection of processor element clock speed;

deriving a chip select restriction signal from the processor speed selection signal and timing signals within said processor element; and

gating chip select signals communicated to the peripheral devices with the chip select restriction signal to modulate the active periods of the peripheral devices to provide for reduced levels of power consumption.

55. A method as recited in claim 54, wherein the duration of the chip select restriction signal is derived from a timer circuit triggered by timing signal within said processing element.